



Form 1449 (Modified) Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Atty Docket No. NOVLP091/NVLS-2889 Applicant: Wu et al. Filing Date April 7, 2004 Application No.: 10/820,525 Group 2823
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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
/J.M./	A1	7,094,713 B1	08.22.06	Niu et al.			
	A2	6,306,564	10.2001	Mullee, William H.			
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	A4	6,149,828 A	11.2000	Vaartstra, Brian A.			
	A5	6,943,121 B2	09.2005	Leu et al.			
	A6	2004/0102032 A1	05.2004	Kloster et al.			
	A7	2006/0197881	09.2006	Kang et al.			
	A8	6,331,480	12.2001	Tsai et al.			
	A9	4,968,384	11.1990	Asano, Akihiko			
	A10	5,648,175	07.1997	Russell et al.			
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Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
/J.M./	C1	U.S. Office Action mailed September 8, 2006, from U.S Application No. 10/404,693 [Atty Dkt No. NOVLP064/NVLS-794].
/J.M./	C2	U.S. Office Action mailed July 12, 2006, from U.S Application No. 10/672,305 [Atty Dkt No. NOVLP069/NVLS-2821].
/J.M./	C3	Wu et al., "Methods for Fabricating High Hardness/Modules Low Dielectric Constant Materials," Novellus Systems, Inc., Appln No. 11/369,658, filed March 6, 2006, pp. 1-33. [NOVLP148/NVLS-3111]
/J.M./	C4	Dhas et al., "Method of Reducing Defects in PECVD TEOS Films," Novellus Systems, Inc., Appln No. 11/396,303, filed March 30, 2006, pp. 1-21. [NOVLP160/NVLS-3168]
/J.M./	C5	U.S. Office Action mailed October 18, 2006, from U.S Application No. 10/849,568 [Atty Dkt No. NOVLP083/NVLS-2867].
/J.M./	C6	Hoek et al., "VLSI Fabrication Processes for Introducing Pores Into Dielectric Materials," Novellus Systems, Inc., Appln No. Not yet assigned, Filed November 28, 2006, pages 1-35. [NOVLP100C1/NVLS-2956C1]
Examiner /Julio Maldonado/		Date Considered 03/21/2007

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.